## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A liquid crystal display device having an ESD protection circuit comprising:

a source electrode and a drain electrode formed on an insulating substrate via an interlayer insulating film;

a gate insulating film having a plurality of hollow portions over said source electrode and said drain electrode to provide a relatively thin film portion partially on said source electrode and said drain electrode and a relatively thick film portion between said source electrode and said drain electrode; and

a gate bus layer formed on said gate insulating film including at least said thin film portion,

wherein an MIM structure is configured by said source electrode, said drain electrode, said gate insulating film in said thin film portion and said gate bus layer.

2. (Original) The device as claimed in claim 1, wherein a plurality of said MIM structures are connected in series.

3. (Original) The device as claimed in claim 1, wherein said thin film portion has a thickness of 50 nm or less.

4. (Currently Amended) A method for manufacturing a liquid crystal display device having an ESD protection circuit comprising the steps of:

forming a source electrode and a drain electrode on an insulating substrate via an interlayer insulating film;

forming a gate insulating film having a plurality of hollow portions over said source electrode and said drain electrode to provide a relatively thin film portion partially on said source electrode and said drain electrode and a relatively thick film portion between said source electrode and said drain electrode; and

forming a gate bus layer on said gate insulating film including at least said thin film portion,

wherein an MIM structure is configured by said source electrode, said drain electrode, said gate insulating film in said thin film portion and said gate bus layer.

5. (Currently Amended) The method as claimed in claim 4, wherein said step of forming said thin film portion in said gate insulating film includes the steps of:

forming an organic film on said gate insulating film;

exposing said organic film using a mask for which the amount of exposure in said thin film portion is relatively low, developing the exposed organic film;

exposing said gate insulating film in said thin film portion by reducing the thickness of the developed organic film; and

forming [[a]] said hollow ~~portion~~ portions by etching said exposed gate insulating film.

6. (Original) The method as claimed in claim 5, wherein said mask includes a portion having a relatively large amount of exposure, said organic film is exposed through said portion, and a contact-hole is formed in a region where the exposed organic film is developed.

7. (Original) The method as claimed in claim 5, wherein a half-tone mask or a diffraction mask is used as said mask for which an amount of exposure in said thin film portion is relatively low.

8. (New) The device as claimed in claim 1, wherein said plurality of hollow portions are formed directly above said source electrode and said drain electrode.

9. (New) The device as claimed in claim 1, wherein said gate insulating film has a larger thickness in areas without the source electrode and the drain electrode formed thereon than areas with said source electrode and said drain electrode formed thereon.